



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/222,524	12/28/1998	SHUICHI MATSUDA	NEC-N98039	3038

7590 05/31/2002

NORMAN P SOLOWAY
HAYES SOLOWAY HENNESSEY GROSSMAN &
HAGE
175 CANAL STREET
MANCHESTER, NH 03101

EXAMINER

PAREKH, NITIN

ART UNIT PAPER NUMBER

2811

DATE MAILED: 05/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. 09/222,254

Applicant(s)

Matsuda

Examiner

Nitin Parekh

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Mar 11, 2002
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-56 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some* c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 7 and 1 6) ☐ Other:

Art Unit: 2811

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Rostoker (US Pat. 5399898) and Liang (US Pat. 5952726).

Regarding claims 21 and 45, the APA discloses a semiconductor device comprising:

- a wiring substrate/tap automated bonding (TAB) substrate/film carrier having a predetermined pattern of wiring formed on one surface and having a number of through-holes
- a semiconductor chip disposed on the other surface of the wiring substrate having chip electrodes and a wiring layer
- a number of bumps formed respectively in through-holes in conforming relationship with the chip electrodes and electrically connecting the wiring with the electrode, and

Art Unit: 2811

- an external bump pad electrically connected through the wiring layer to the chip electrodes.

The admitted prior art fails to specify the semiconductor chip having two or more chip electrodes in a common wiring layer and arranging them from the edge of the chip towards it's inner side.

Rostoker teaches using a semiconductor chip comprising a variety of internal connections and having an electrode set comprising two electrodes (222 c and d in chip 224; Fig. 2b) being connected to a common wiring layer (Fig. 2b; Col. 11, line 23- Col. 12, line 13) in a flip-chip assembly. Rostoker further teaches increasing the bond pad/bump density using conventional bond size/spacing to 600 or 1000 I/O counts or more to achieve the desired external connection capability and increased bump connections for a given chip area (Fig. 6-7B; Col. 17, line 20- Col. 19, line 35).

Liang teaches using a conventional grid/pattern of chip electrodes/bump pads comprising ground, power-source and signal terminals in a in a flip-chip assembly having a variety of configurations with different parameters such as pitch/dimension, number of electrodes, etc. where the chip electrodes/pads are arranged from the edge of the chip towards it's inner side or parallel to the edge of the chip (Fig. 2: Col. 1, line 42; Col. 2, line 42; Fig. 4-6; Col. 5, line 1-45; Col. 2-5).

Art Unit: 2811

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate a chip having an electrode set or two electrode sets comprising two electrodes in a common wiring layer in the semiconductor chip and arranging them from the edge of the chip towards its inner side so that the internal connection density and bump stress distribution can be improved using Rostoker and Liang's design in the admitted prior art.

Regarding claims 24, 27, 30, 33, 36, 39, 42, 48, 51 and 54, as explained above for claims 21 and 45, the admitted prior art fails to specify the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip.

Liang teaches using the chip electrodes comprising ground, power-source and signal terminals of the semiconductor chip in a flip-chip assembly (Fig. 4A-C; Col. 2-9; Fig. 1-7).

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the chip electrodes comprising at least one kind of terminal selected from ground, power-source and signal terminals of the semiconductor chip so that the desired grounding and power/signal routing can be achieved using Liang's design in the admitted prior art in view of Rostoker.

Art Unit: 2811

3. Claims 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Rostoker (US Pat. 5399898), Liang (US Pat. 5952726) and further in view of Fulcher (US Pat. 5686764).

Regarding claims 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52 and 55, the admitted prior art fails to show an arrangement of the chip electrodes being parallel to an edge of the chip and the wiring being bent at least one position.

As explained above for claims 21, 24 and 45, Rostoker teaches using a semiconductor chip comprising a variety of internal connections and having the chip electrode sets comprising two electrodes (222 c and d in chip 224; Fig. 2b) being connected to a common wiring layer (Fig. 2b; Col. 11, line 23-Col. 12, line 13) in a flip-chip assembly.

Liang teaches using a conventional grid/pattern of chip electrodes/bump pads comprising ground, power-source and signal terminals in a in a flip-chip assembly having a variety of configurations with different parameters such as pitch/dimension, number of electrodes, etc. where the chip electrodes are arranged from the edge of the chip towards it's inner side or parallel to the edge of the chip (Fig. 2: Col. 1, line 42; Col. 2, line 25-55; Fig. 4A-D; Col. 3, line 60- Col. 7, line 65). Liang further teaches using power/signal wiring layout with patterns of different dimensions, shapes where

Art Unit: 2811

the wiring is bent at various positions (Fig. 4A; Col. 7, line 10) to achieve the desired power/signal routing (Fig. 1-4, Col. 3-9).

Fulcher teaches using I/O, power/signal wiring layout with patterns of different dimensions, shapes where the wiring is bent at various positions (Fig. 4A; Col. 7, line 10) in a flip chip substrate/tape to optimize the spacing of wiring/traces and to reduce the signal interference and cross-talk (Fig. 3-8, Col. 3-5).

Therefore, it would have been obvious to a person of ordinary skill in the art to select an arrangement of the chip electrodes where they are arranged parallel to an edge of the chip and the wiring is bent at least one position so that the spacing of wiring/traces can be optimized and the signal interference/cross-talk can be reduced using Fulcher's substrate design in the admitted prior art in view of Rostoker and Liang.

4. Claims 23, 26, 29, 32, 35, 35, 38, 41, 44, 47, 50, 53 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Rostoker (US Pat. 5399898), Liang (US Pat. 5952726) and further in view of Fulcher (US Pat. 5686764) and Bertolet et al (US Pat. 5844317).

Regarding claims 23, 26, 29, 32, 35, 35, 38, 41, 44, 47, 50, 53 and 56, the admitted prior art fails to specify the chip electrodes being parallel to an edge of the chip and the

Art Unit: 2811

wiring having an end width larger than an interelectrode distance between the chip electrodes.

As explained above for claims 21, 22, 24 and 45, the APA in view of Rostoker, Liang and further in view of Fulcher teach using a variety of arrangements and shapes/dimensions of electrode layout and wiring patterns.

Bertolet et al teach using a variety of shapes/dimensions and end widths of wiring pattern/pad (Fig. 3) to achieve the desired bonding area and to improve the bonding strength.

Therefore, it would have been obvious to a person of ordinary skill in the art to select an arrangement of the chip electrodes where they are arranged parallel to an edge of the chip and the wiring dimension which has an end width larger than an interelectrode distance between the chip electrodes so that the desired bonding area, bonding strength and bump stress distribution can be achieved using Fulcher and Bertolet et al's substrate designs in the admitted prior art in view of Rostoker.

Response to Arguments

5. Applicant's arguments filed on 03-11-02 have been fully considered but they are not persuasive.

Art Unit: 2811

A. Applicant contends that Rostoker teaches three electrodes connected to a common layer and teaches using jumper contacts.

However, as explained above, Rostoker teaches using a semiconductor chip comprising a variety of internal connections and having an electrode set comprising two electrodes (222 c and d in chip 224; Fig. 2b) which are connected to a common wiring layer (Fig. 2b; Col. 11, line 23-Col. 12, line 13). Furthermore, the jumpered contacts/connections in Rostoker comprise chip electrode set/electrodes/bumps being connected in a common wiring layer providing increased I/O density, improved routing and higher bonding strength.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

Art Unit: 2811

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

05-22-02


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800